Multilevel two quadrant DC/DC converter for regenerative braking in mobile applications

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Keywords

<<Power converters for HEV>> <<Power converters for EV>> <<Multilevel converters>> <<DSP>> <<Charge compensation device>> <<SC>> << Modulation strategy>>

Abstract

In this paper different cascaded and multilevel topologies are compared for regenerative braking systems using supercapacitors (SC). It shows that the multilevel buck derived topology can beneficiate from both reduced voltage across the inductor and increased frequency to reduce the output inductance, even if there is the need for an input LC filter to reduce harmonic content in the SC. Also, the proposed control scheme is able to control the energy flow between SC and the DC bus, balancing the voltage in the SC banks. Experimental results verify the performance of the proposed converter and its control algorism.

Introduction

This proposal underlines the need for low volume, low weight and high efficient converters for mobile application, where these properties are critical. There are numerous uses [1], but the most interesting ones are the design small, high efficient converters for electric vehicles (EV) and hybrid electric vehicles (HEV).

System efficiency is one of the main objectives in mobile electric applications [2][3]. Using power electronic devices, the increase in energy efficiency can be a double purpose, more efficient energy management and weight (and volume) reduction.

The main advantage of using electric traction is that the motor used is energy reversible, and the braking energy can be stored for future use, instead of being dissipated as in traditional mechanical braking systems. Therefore, a converter for that purpose is needed.

Batteries and SC are mainly used in mobile applications as storage devices instead of flywheels and superconductive magnetic storage systems because there are no moving components but also control systems are simpler. But for high energy dynamics, as in regenerative braking applications, SC are preferred to batteries because of their higher power density and reliability [4].

SC are low voltage devices. To achieve the high voltages needed in traction applications, a large number of elements must be connected in series. Direct series connection of SC of different capacitance value can lead to voltage imbalances between cells because of the common series current. These voltage imbalances can produce overvoltage and destruction of cells. Passive and active power electronics based devices have been proposed in the literature to balance cells voltage [5].

Also, SC capacity performance degrades for frequencies of current above 100 Hz, where the capacitance value is near zero, and behaves as a resistor, producing only losses, reducing its lifetime.

It must be stated that multilevel converters offer several advantages over conventional converters. The first one is the reduction of the voltage across the inductor, splitting one inductance into small inductances. Splitting the converter into several converters also reduces the voltage rating of the transistors. Low voltage transistors can achieve higher switching frequencies, and higher current capability. Another important advantage is modularity that can simplify system design and cooling, and can increase reliability in $N + 1$ redundant system. Independent energy management can be achieved for each of the low voltage sources. Multilevel converter topologies are a good trade-off solution between performance and cost, as control complexity increases compared to traditional converters [6][7].

Design of the multilevel converter

Different multilevel topologies are discussed to obtain the best relationship between size and number of cells, but all these topologies are based on the half bridge two quadrant DC/DC converter [8] as shown in Fig.1.

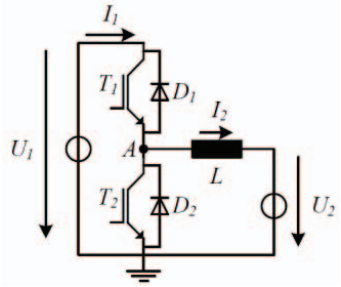

Fig.1: Two quadrant DC/DC cell.

In the half bridge converter, the relationship between U_1 and U_2 is described in Eq. (1), where D is the duty cycle of the converter.

$$U_1 \cdot D = U_2 \tag{1}$$

The output inductor can be calculated as depicted in Eq. (2).

$$L_{CBk} = \frac{U_1 \cdot (1 - D) \cdot D}{\Delta I_2 \cdot f_s} \tag{2}$$

Depending on the connection point of SC and connection of cells, three topologies can be derived: cascaded buck, cascaded boost and multilevel buck topology [9][10]. These are shown in Fig.2.
To determine the proper number of series connected cells, the magnetic energy stored in the inductances for the three topologies can be compared. Magnetic energy stored is related to the overall size and weight of the converter, but it's mostly related to the size of the inductor needed. Minimizing magnetic energy means saving money and reducing size and weight.

Comparison of different topologies

For buck derived topologies and due to input harmonic currents, an LC filter must be added in order not to degrade SC performance. This LC filter increases the number of magnetic elements.
The three topologies are compared assuming constant inductor current ripple, constant frequency, and a filter inductor value of 1% of the one cell output inductor.
For Cascaded Buck Topology (CBk), U_2 is the DC bus voltage and U_1 is the sum of all the SC voltages. When $U_1 = 2 \cdot U_2$ ($D = 0{,}5$), Equation (3) can be written.

$$L_{CBk} = \frac{U_1 \cdot (1 - D) \cdot D}{\Delta I_2 \cdot f_s} = \frac{U_1 \cdot (1 - 0{,}5) \cdot 0{,}5}{\Delta I_2 \cdot f_s} \tag{3}$$

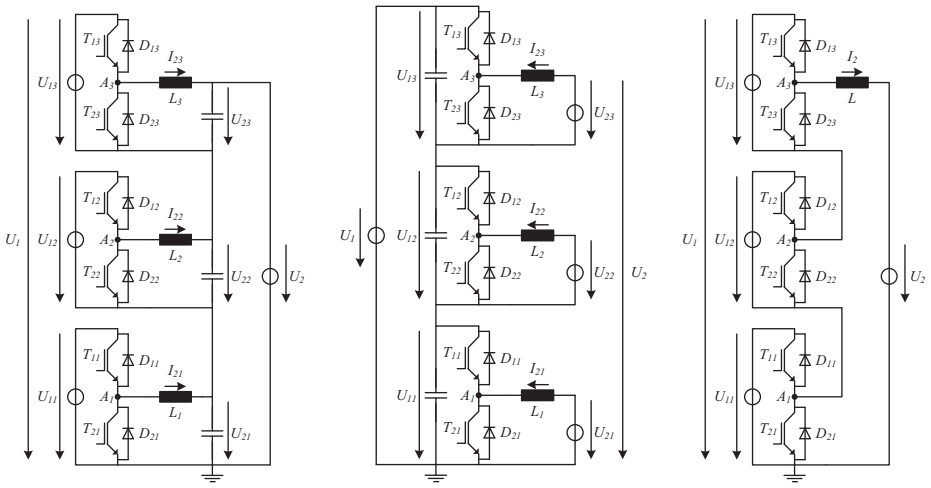

Fig.2: (From left to right) Cascaded buck, cascaded boost and multilevel buck three level converters.

So the magnetic energy stored is obtained by Eq. (4).

$$E_{CBk} = \frac{1}{2} L_{CBk} I_2^2 \tag{4}$$

And if it is assumed that the energy stored in the filter is equal to 1% of the energy stored in the output inductance for one level converter, then Eq. (5) can be written for N levels.

$$E_{CBk} = \frac{1}{2} L_{CBk} I_2^2 + 0{,}01N \frac{1}{2} L_{CBk} I_2^2 \tag{5}$$

And then, this energy is divided in N inductors.
For the Cascaded Boost converter, SC voltages are U_{2N} and the DC bus voltage is U_1. Notice that in this topology, to maintain the same power when the SC voltages are the half, current has to double. So the current ripple through the inductance is also doubled as shown in Eq. (6) when $U_1 = 2 \cdot U_2$.

$$L_{CBt} = \frac{U_2 \cdot (1 - D) \cdot D}{\Delta I_2' \cdot f_s} = \frac{U_1 \cdot (1 - 0{,}5) \cdot 0{,}5}{4 \cdot \Delta I_2 \cdot f_s} \tag{6}$$

The relationship between these two inductances is shown in Eq. (7).

$$\frac{L_{CBk}}{L_{CBt}} = \frac{4}{1} \tag{7}$$

Although the inductance value is for times smaller, the energy stored is the same that in the cascaded buck output inductance.

$$E_{CBt} = \frac{1}{2} \frac{L_{CBt}}{N} N I_2'^2 = \frac{1}{2} \frac{L_{CBk}}{4} (2I_2)^2 \tag{8}$$

$$E_{CBt} = \frac{1}{2} L_{CBk} I_2^2 \tag{9}$$

If the same inductor current ripple had to be kept constant ($\Delta I_2 = cnt$), then Eq. (10) can be written.

$$L_{CBt(\Delta I_2 = cnt)} = 2 \cdot L_{CBt} \Longrightarrow E_{CBt} = \frac{1}{2} L_{CBt(\Delta I_2 = cnt)} I_2^2 = 2 \cdot E_{GBt} \tag{10}$$

For the Multilevel Buck converter, the inductance is the same as in the Cascaded Buck for the first level, but when the number of levels increase and a phase shifting strategy is used, Eq. (2) is no longer valid [11], the inductance has to be calculated as depicted in Eq. (11).

$$L_{MBk} = \frac{(U_{max} - U_{min}) \cdot \left(1 - D_{eqmax}\right) \cdot D_{eqmax}}{\Delta I_2 \cdot f_{eq}} = \frac{U_1 \cdot (1 - 0{,}5) \cdot 0{,}5}{\Delta I_2 \cdot f_s \cdot N^2} \tag{11}$$

where,

- $\mathrm{D_{eqmax}} = \mathrm{N} \cdot \mathrm{D} \bmod \left(\frac{1}{\mathrm{N}}\right)$ is the equivalent duty cycle at the point A_3 where the maximum ripple occurs.
- $\Delta \mathrm{I_2}$ is the output inductor ripple.
- $f_{\mathrm{eq}} = \mathrm{N} \cdot f_{\mathrm{s}}$ is the equivalent frequency (f_{s} is the switching frequency).
- N is the number of series connected converters.
- U_{max} and U_{min} are the maximum and the minimum voltages at the A_3 point in Fig 2. These voltages can be calculated by Eq. (12) and (13).

$$\mathrm{U_{max}} = \mathrm{N} \cdot \mathrm{U_{1N}} \left[\mathrm{D} - \mathrm{D} \bmod \left(\frac{1}{\mathrm{N}}\right) + \frac{1}{\mathrm{N}}\right] \tag{12}$$

$$\mathrm{U_{min}} = \mathrm{N} \cdot \mathrm{U_{1N}} \left[\mathrm{D} - \mathrm{D} \bmod \left(\frac{1}{\mathrm{N}}\right)\right] \tag{13}$$

- $\mathrm{U_{1N}} = \mathrm{U_1}/\mathrm{N}$ is the one converter input voltage and D is the working duty cycle.

The reduction is proportional to the inverse square of the number of cells, so energy is given by Eq. (14).

$$E_{MBk} = \frac{1}{2}\frac{L_{CBk}}{N^2} I_2^2 + 0{,}01 \cdot N \cdot \frac{1}{2} L_{CBk} I_2^2 \tag{14}$$

Finally, rewriting Eq. (5), (9), (10) and (14) the next relationships can be written:

$$\begin{array}{ccc} E_{CBk} & \propto & 1 + 0{,}01 \cdot N \\ E_{CBt(\%I_2 = cnt)} & \propto & 1 \\ E_{CBt(\Delta I_2 = cnt)} & \propto & 2 \\ E_{MBk} & \propto & N^{-2} + 0{,}01 \cdot N \end{array} \tag{15}$$

As can be seen in Fig. 3, the total magnetic energy for the Cascaded Buck converters increases as the number of series connected converters increase because the number of input filters needed increases. On the other hand, the total magnetic energy of the Cascaded Boost remains constant because there is no need for an input filter inductance.

The minimum total magnetic energy is achieved by the Multilevel Buck topology for a six cell converter. This is the proposed topology in this paper. The curve increases from six on because of the SC inductance filter needed in each level.

Control of the multilevel converter

The control objective is the output inductor L current $\mathrm{I_2}$. The reference for this current is fixed for a higher level control system that controls the energy flow between other storage or generation elements and the traction system. This higher level control system is out of focus of this work.

Each cell has its own modulator, and each modulator has its own triangular PWM carrier, but all these carriers are $2\,\pi\,/\,N$ out of phase. That assures the shifted switching operation of the converter.

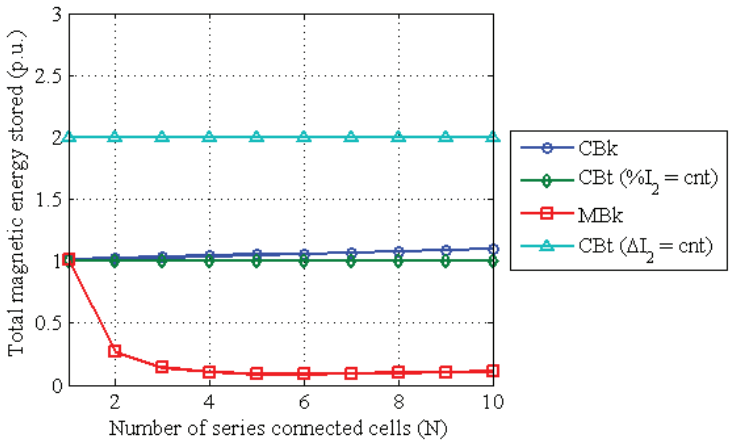

Fig. 3: Total magnetic energy stored as a function of the number of cells for the three proposed topologies.

Regardless of the type of the connection architectures, at least two control loops are needed: one being to regulate the system output voltage and the other being to control the output current. Basically, the two control loops are exercised by varying the duty cycles of the modules. However, varying the duty cycles may affect both the output voltage of the system and the sharing of the output currents of the modules. Thus, the two control loops may be coupled, resulting in difficulties in the design of the loops. But it can be demonstrated that this loops are not coupled [12].
According to Eq. (16), the relationship between the input voltage and the output voltage is

$$D_N U_{1N} = U_{2N} \tag{16}$$

Where d_i is the duty cycle of the *i*-th module, and it's the sum of the two control loops duty cycles

$$D_N = D_{I_2 loop\_N} + D_{U_{1N} loop\_N} \tag{17}$$

Perturbing Eq. (16) leads to Eq. (18).

$$\left(\hat{d} + d_{I_2 loop\_N} + d_{U_{1N} loop\_N}\right)(\hat{u}_{1N} + u_{1N}) = (\hat{u}_{2N} + u_{2N}) \tag{18}$$

Where $\hat{d}$ is the quiescent value of D and d is a small AC perturbation. Multiplying and discarding second order terms, and noting that DC terms on both sides are equal, Eq. (19) can be written.

$$\hat{d} \cdot u_{1N} + d_{I_2 loop\_N} \cdot \hat{u}_{1N} + d_{U_{1N} loop\_N} \cdot \hat{u}_{1N} = u_{2N} \tag{19}$$

Hence, summing all cells from Eq. (19) leads to Eq. (20).

$$\hat{d} \cdot u_1 + \hat{u}_1 \sum_{i=1}^{N} d_{I_2 loop\_N} + \hat{u}_1 \sum_{i=1}^{N} d_{U_{1N} loop\_N} = u_2 \tag{20}$$

It can be seen that if the condition shown Eq (21) is accomplished,

$$\sum_{i=1}^{N} d_{U_{1N} loop\_N} = 0 \tag{21}$$

then, the output voltage variations just depend on the variations of the duty cycle of the output voltage loop. Thus, the voltage stabilization loop can be controlled independently of the main control loop, and the sum of all terms added to the duty cycle has to be zero.

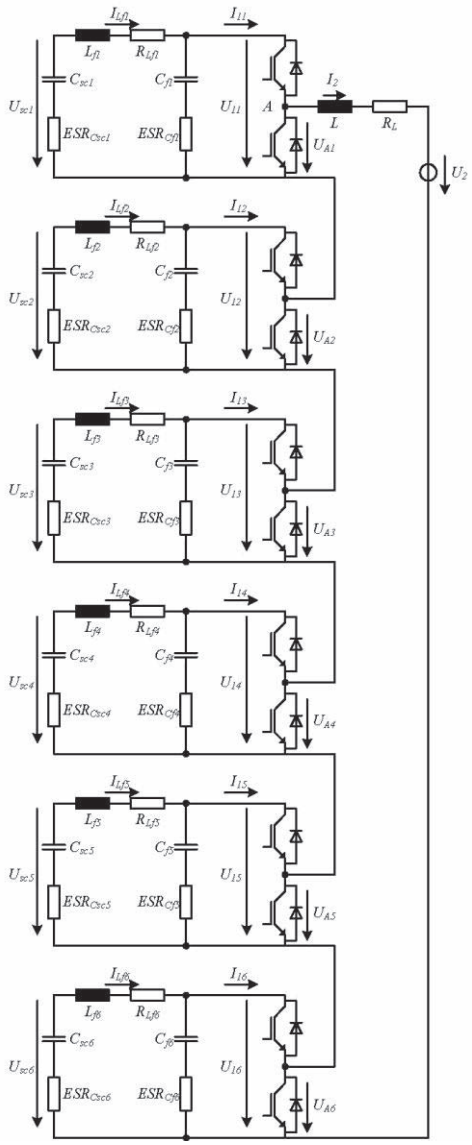

Fig.4: The proposed multilevel modular DC/DC converter.

Output inductor current control loop

For control purposes, the converter can be modeled as single stage, two quadrant converter. The reference current is compared to the output inductor measured current and the difference is fed to a controller. The output of the controlled is modulated with the six PWM modulators to generate the switching signals for the transistors.

This system can be considered a first order R-L system as it is shown in Eq. (22).

$$G_s(s) = \frac{1/R_L}{1 + s\,L/R_L} \tag{22}$$

Then, a PI controller can be used for control purposes, with good performance. PI controller parameters are tuned using IMC method [13],[14]. The constants are selected as shown in Eq. (23).

$$K_p = \alpha \cdot L \qquad K_i = \alpha \cdot R_L \tag{23}$$

Where α is selected to fix the 10% to 90% rise time t_r as

$$t_r = \frac{\ln 9}{\alpha} \tag{24}$$

So that the closed loop transfer function is

$$W(s) = \frac{G_c(s)G_s(s)}{1 + G_c(s)G_s(s)} = \frac{1}{1 + \frac{s}{\alpha}} \tag{25}$$

SC voltage equalization loop

For proper operation of the converter and to equalize the stored energy in SC, it is necessary to balance the voltage of the SC banks. A new compensation loop must be added for this purpose. This compensation loop compares the voltage of the *i*-th SC with the average value of all the SC voltages. A P controller adds some gain to this error. The output of the P controller is added to the duty cycle [15]. With this compensation, the value of each SC will tend to the average value. The controller gain K_{pSC} is determined knowing that the transfer function of the system is a first order capacitor as shown in Eq. (26).

$$G_s = \frac{1}{sC_{SC}} \tag{26}$$

The bode diagram of the system to be controlled is a straight line with -20 dB/decade, that crosses 0 dB at $\omega = 1/C_{SC}$. The controller adds some gain, moving up this line as depicted in Eq. (27),

$$K_{pSC} = 10^{\frac{-3}{20}} \cdot \frac{\omega_c}{\frac{1}{C_{SC}}} \cdot sign(I_2) \tag{27}$$

where ω_c is the desired bandwidth of the closed loop system. This bandwidth must be chosen low enough not to perturb the current loop and to limit SC currents when compensating SC voltages. Also, the output current sign matters because this compensation has to be added when SC are discharging and subtracted when SC are charging.
Hence, it is not necessary that cells have the same voltage since the control will drive the required energy depending on the charge of each cell, matching all charges to the relative total charge [16].

Semiconductor voltage drop compensation

Since the number of semiconductors grow as more cells are connected, a new term is added to the control effort to compensate the semiconductors voltage drop. This voltage drop is added to the output, and the sign is selected depending on the output current. The final control scheme can be seen in Fig.5.

Simulation results and experimental verification

A model has been programmed and simulated with Matlab and Simulink, and it has been compared to the experimental results. Six half bridge converters with a SC bank in them have been connected in series, and are controlled with a DSP TMS320F2808 of Texas Instruments. Measurements of the six voltages and one current are fed into the ADC of the controller and are used for control purposes. The DSP outputs, which are the PWM signals, are then driven to their respective boards. In Fig. 6 the experimental setup is shown.
The specifications of the experimental setup are:

- DC bus voltage: 12 V
- SC bank voltage: 16,2 V
- Nominal current: 5 A
- Switching frequency: 20 kHz
- Output current frequency: 120 kHz
- SC Banks capacity: 58,3 F/cell
- Balancing loop bandwidth: $\omega_c = 5/C_{sc}$
- Rise time: $t_r = 0{,}4\ ms$

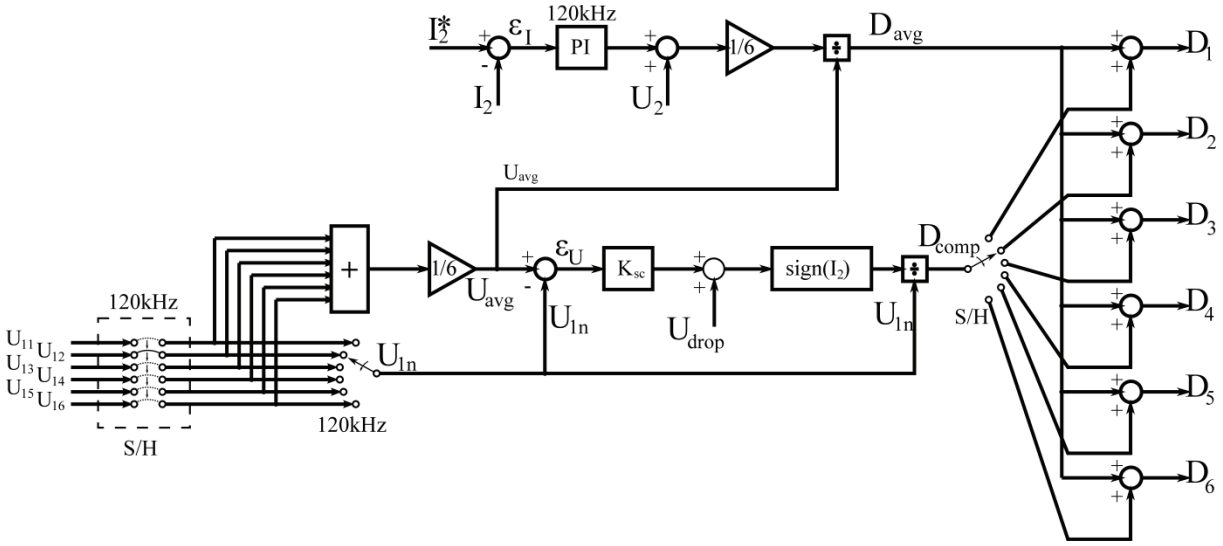

Fig.5: Control diagram of the multilevel converter.

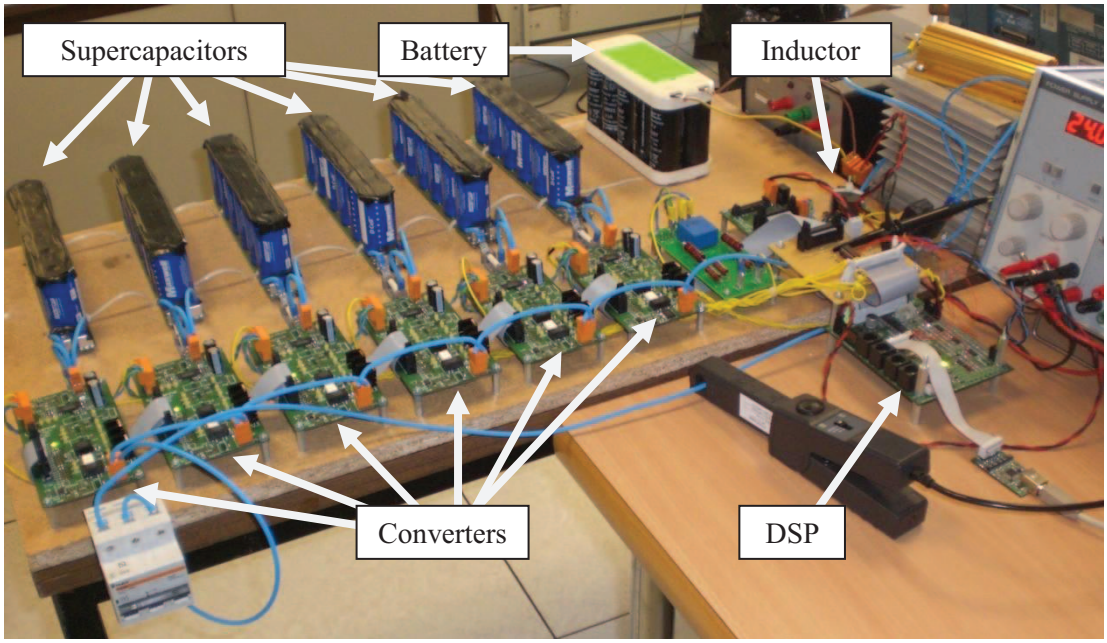

Fig. 6: Experimental setup.

The control algorithm is executed every time a new measurement is converted in the ADC module of the DSP. Current measurements are renewed at 120 kHz frequency and cells voltages at 20 kHz, but in different time, so every new measured current comes with a new cell voltage, one at a time. Therefore, when the current measurement has been renewed six times, the voltages of all the cells have been renewed and the voltage balancing loop can be executed.

In Fig. 7 the output current response to a -5 to 5 A set point value is shown, with a rise time of 0,4 ms as expected, and in Fig. 8 open loop output current is shown and compared to a 20 kHz PWM signal to show the 120 kHz frequency of the current.

In Fig. 9 voltage balancing loop is shown, where it can be seen that the voltages of all cells converge in the same value. The voltage decreases due to the internal resistance of the battery connected to the DC bus and also due to the internal resistance of the SC cells.

Conclusions

A multilevel two quadrant DC/DC converter has been built and tested with good performance. The output current response is not only fast but without oscillations as neither with overshoot. It can be used for regenerative braking as well as many other mobile applications. The voltage balancing loop achieves its purpose in keeping the voltage in control. Experimental results were also presented and corresponded well to the theoretically predicted results and justify the theoretical analysis.

The phase shifting strategy reduces the inductance value needed for a constant ripple, so a lighter converter can be build and keep the same performance or even a better one. Unfortunately, the control of the converter is more complex compared to converters without this control strategy.

Thanks to the voltage control loop, all the capacitors share the same voltage, which makes the circuit easy to control and suitable for various power applications.

Multilevel buck derived topology excel in low volume and weight given that the frequency can be higher due to shifted switching commutation strategy, and a much smaller inductance is achieved maintaining the same current ripple, lowering the system weight and volume.

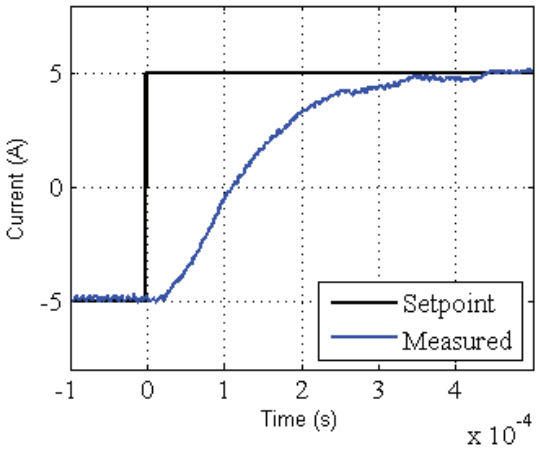

Fig.7: -5A to 5A step response.

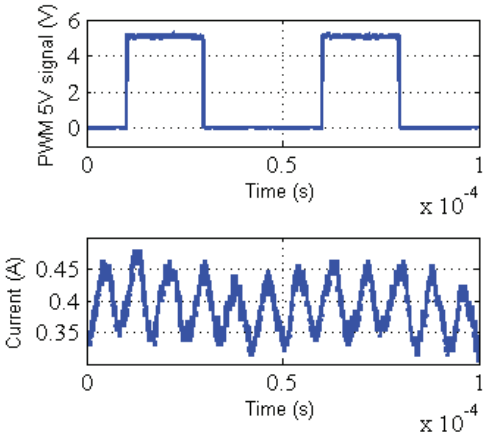

Fig. 8: 120kHz output current

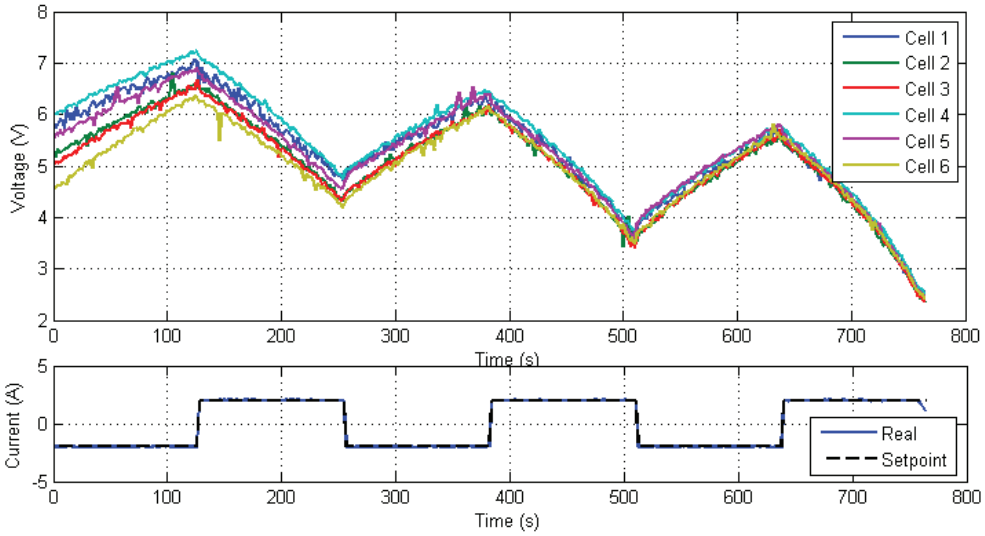

Fig. 9: Charge and discharge of the SC banks, balancing their voltages.

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