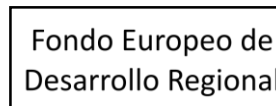


A First Performance Analysis of the Admission Control in the HaRTES Ethernet Switch

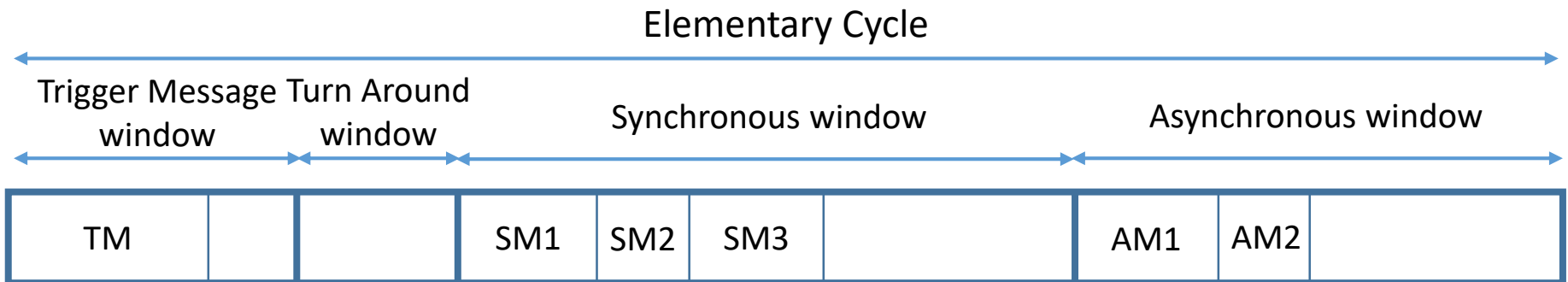
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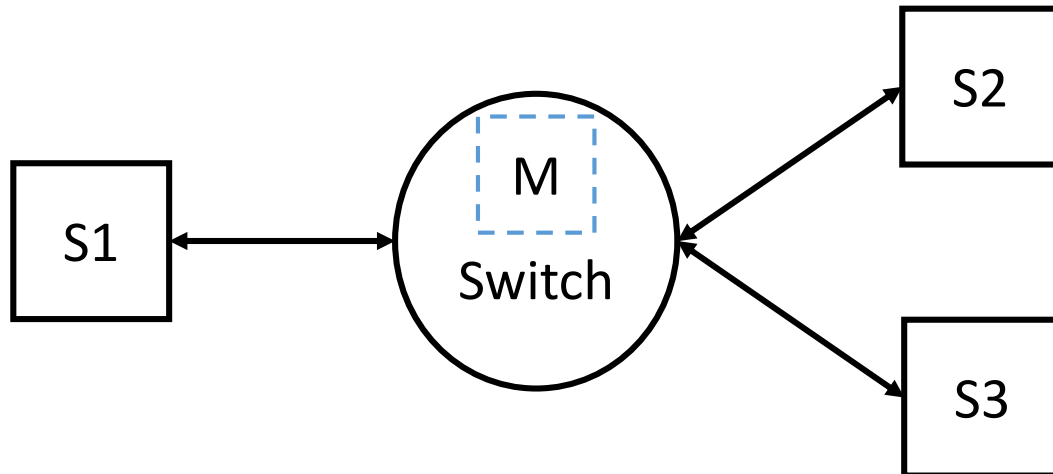
Flexible Time-Triggered

- **Time-triggered** and **event-triggered** traffic.
- Master/multi-slave architecture.
- Communication divided in **Elementary Cycles**.



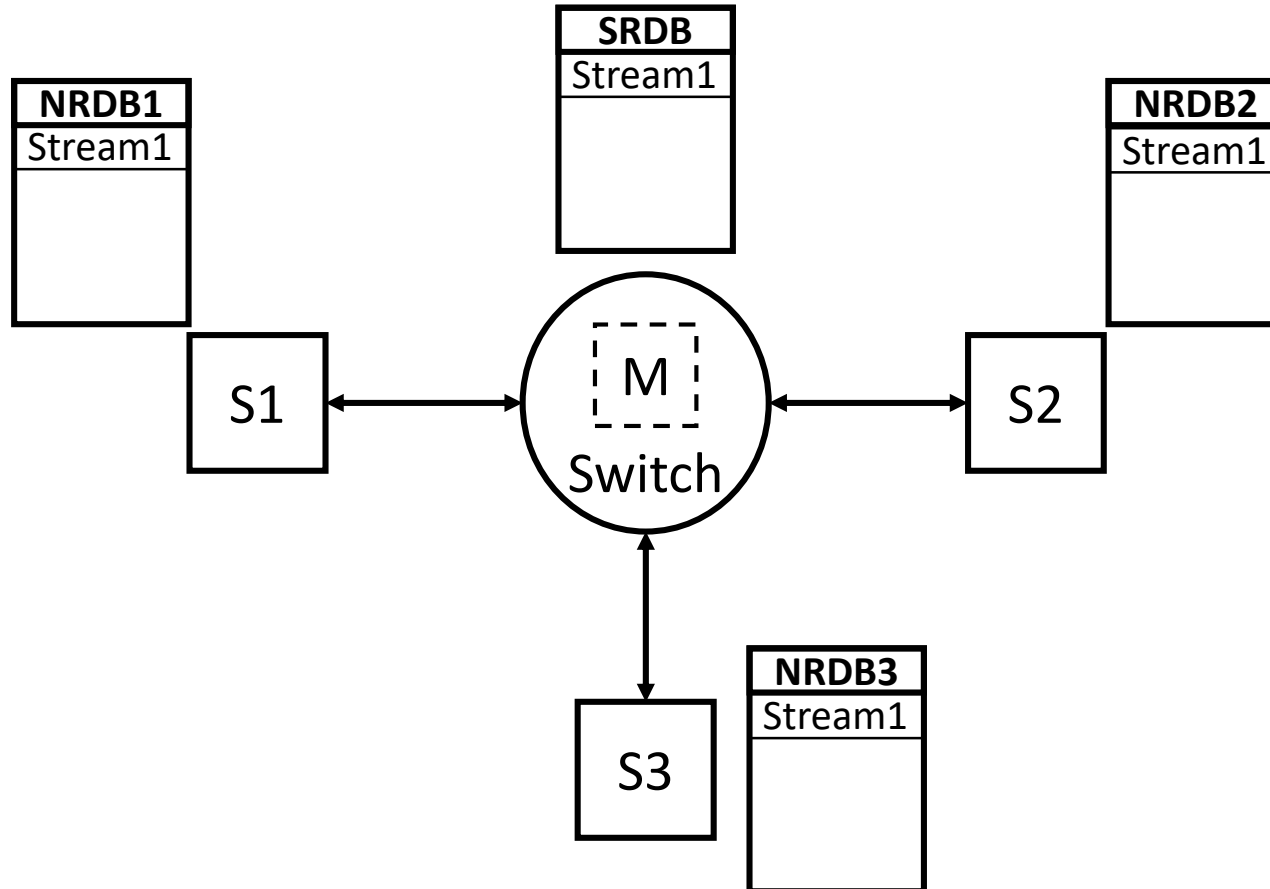
Flexible Time-Triggered

- **HaRTES** architecture: master inside the switch.
- Communication done through **streams**.
- Slaves can request changes in streams → **Admission Control**.



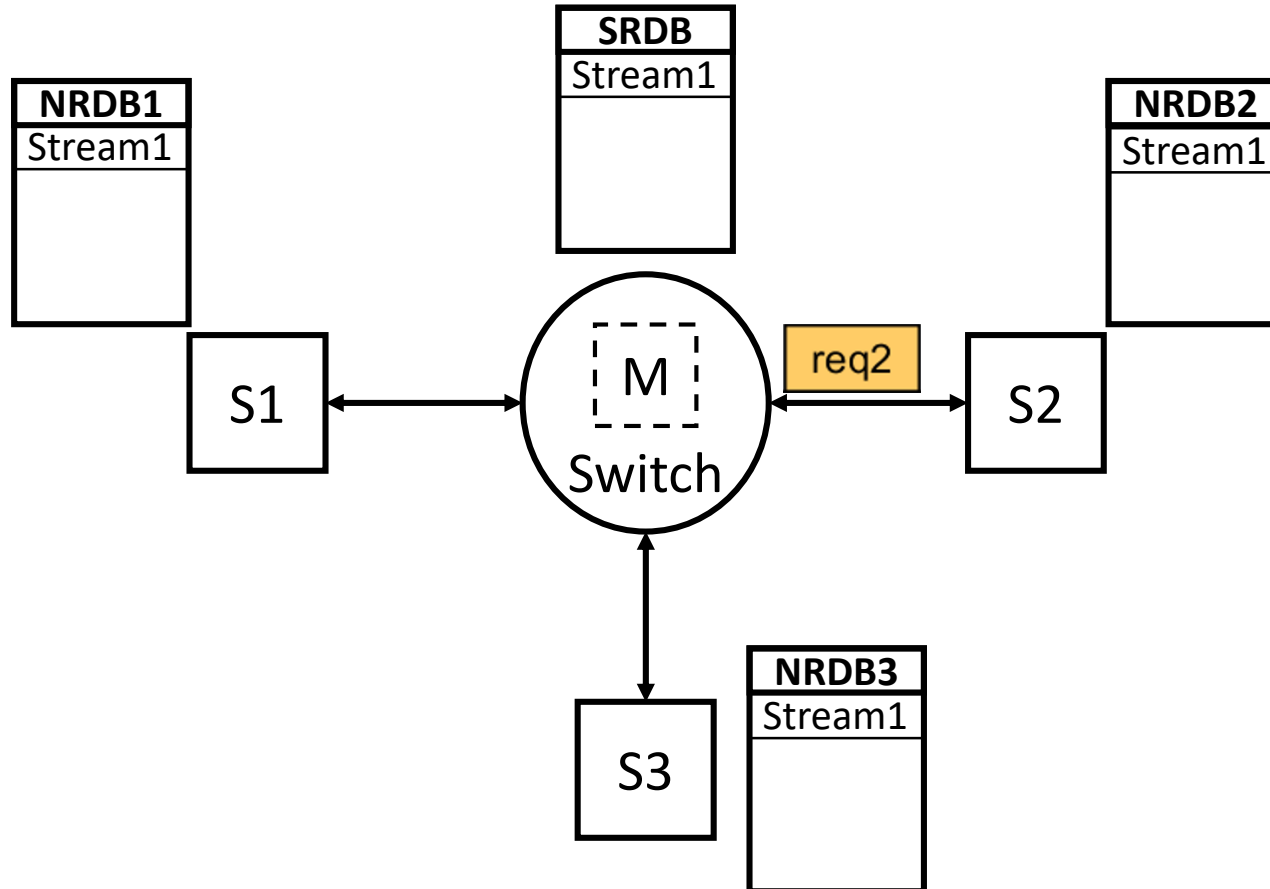
Admission Control

Stream information in **SRDB** and **NRDBs**



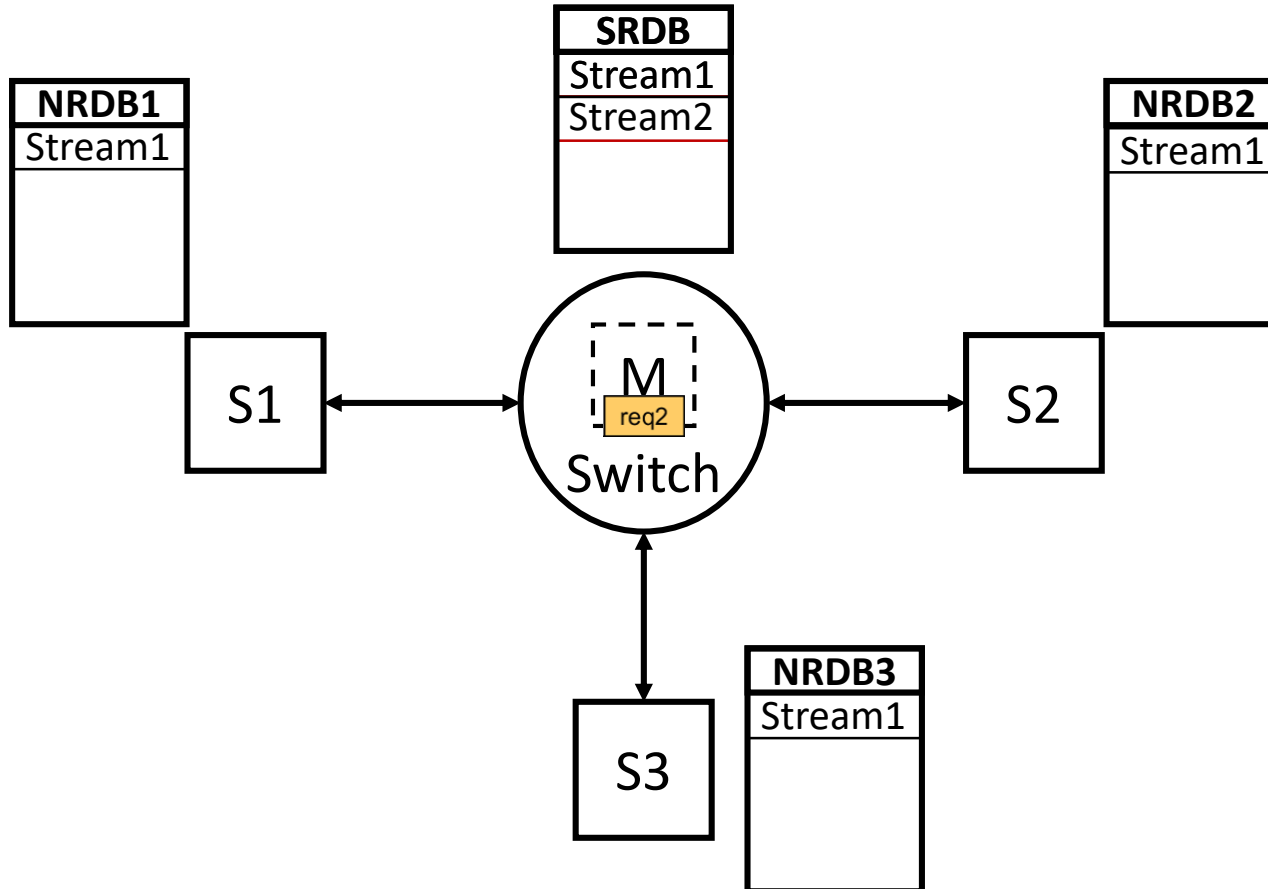
Admission Control

Slave sends **request** to the Master



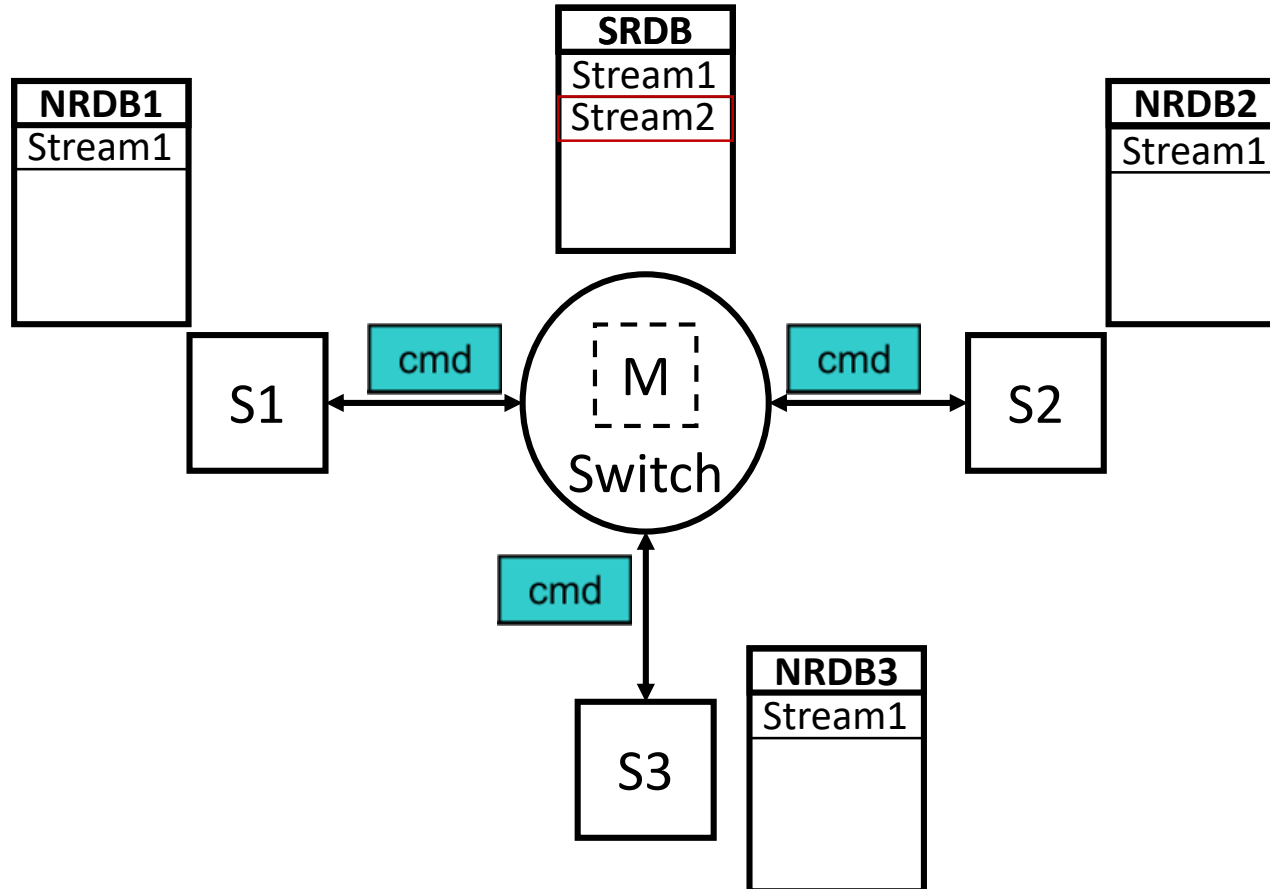
Admission Control

Master **processes** the request



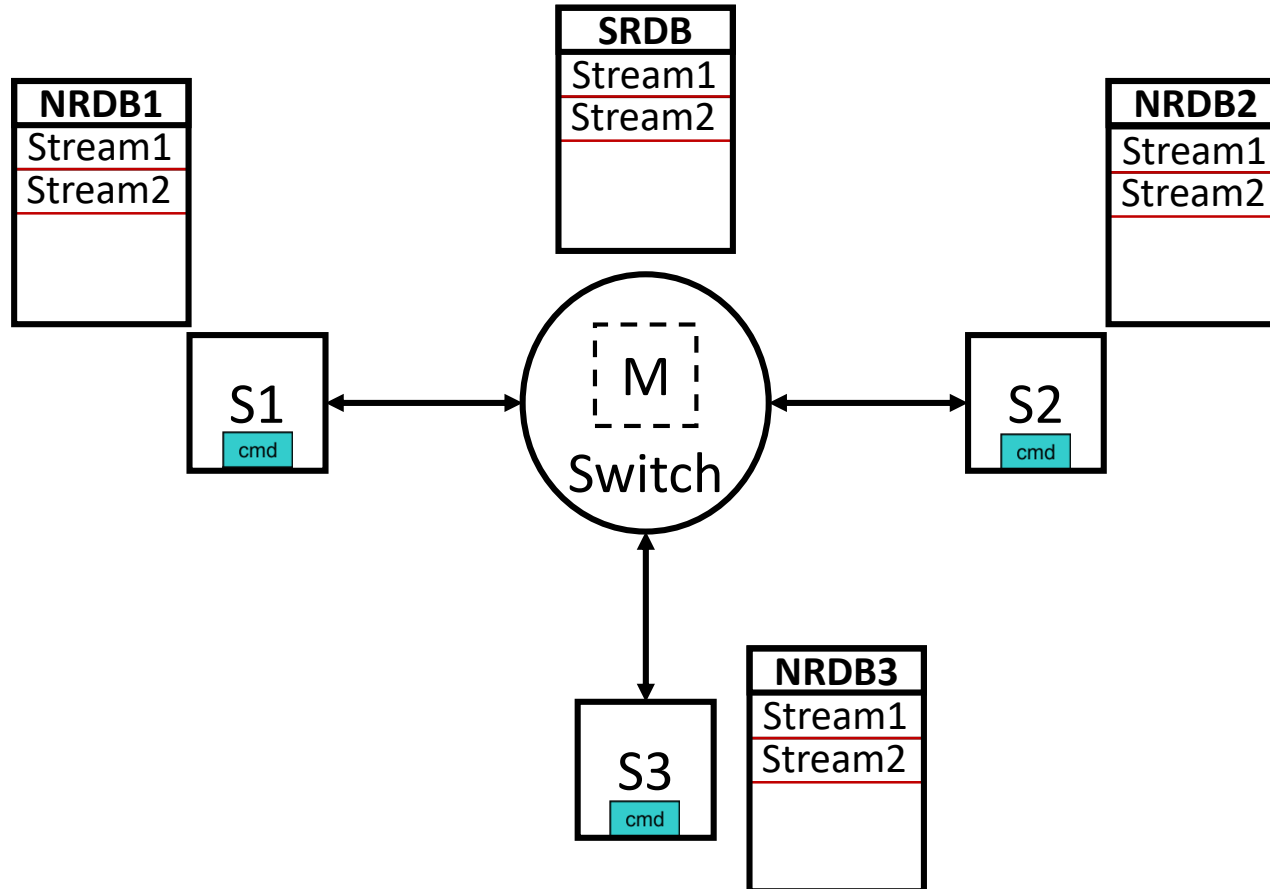
Admission Control

Stream information in NRDBs and SRDB



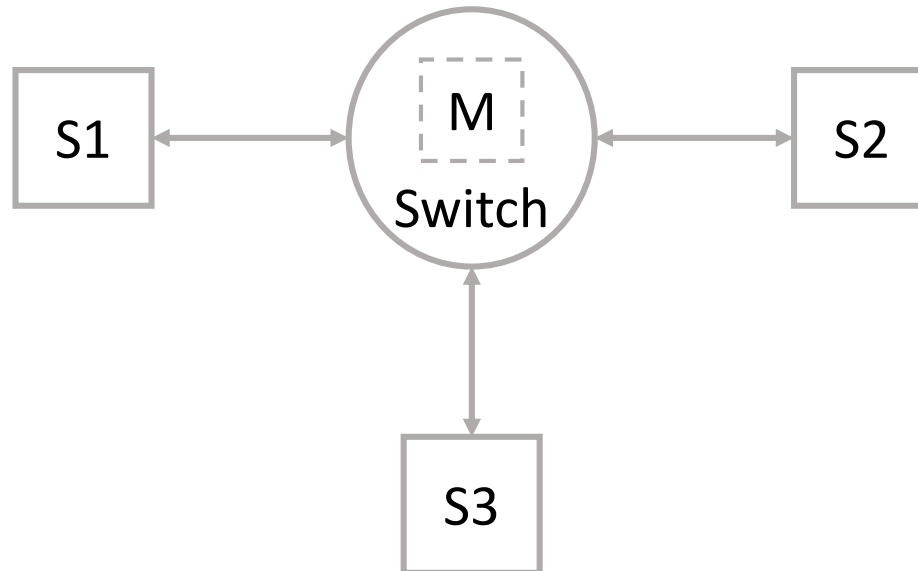
Admission Control

Stream information in NRDBs and SRDB

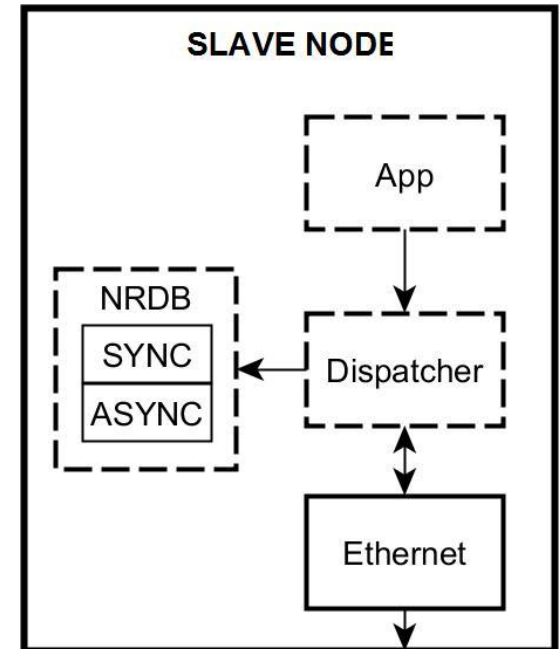
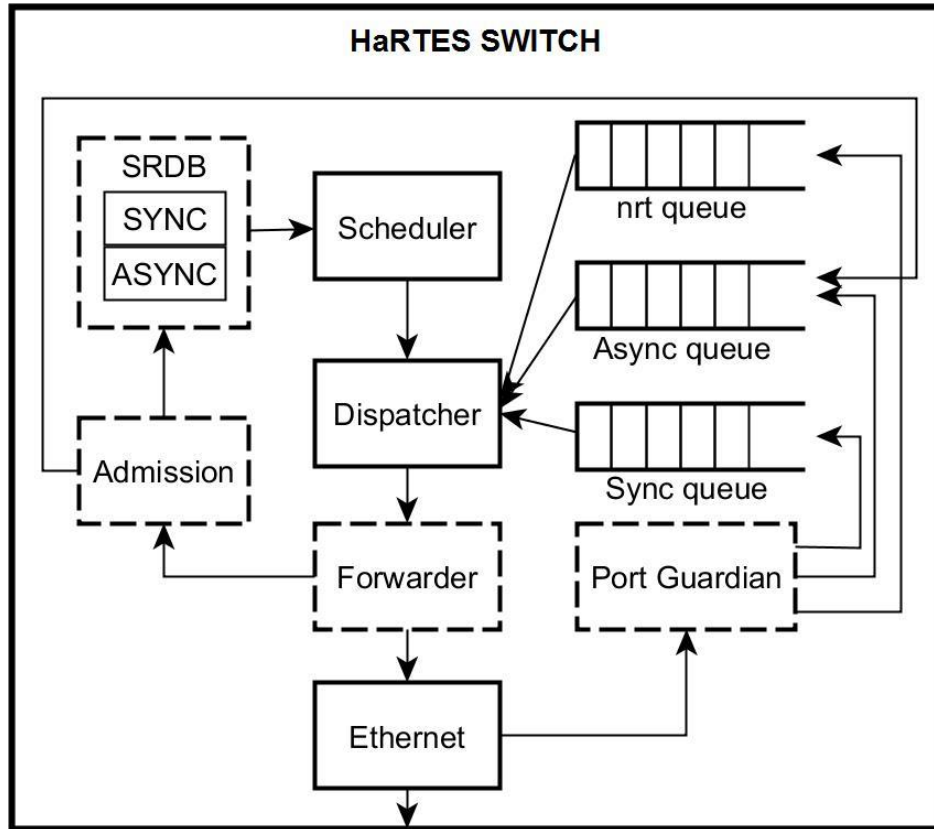


Admission Control Study

Study the performance of the Admission Control process



OMNeT++ Model

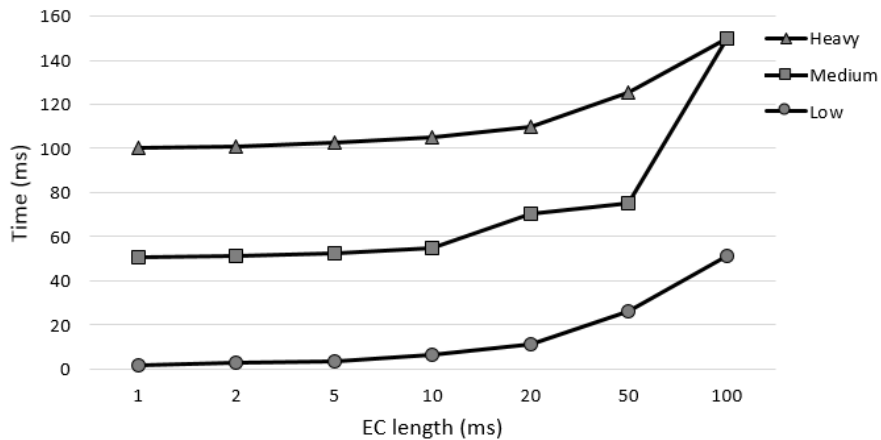


Knezic, M., Ballesteros, A. and Proenza, J., "Towards extending the OMNeT++ INET framework for simulating fault injection in Ethernetbased Flexible Time-Triggered systems," in Proceedings of the 2014 IEEE Emerging Technology and Factory Automation (ETFA), Sept 2014.

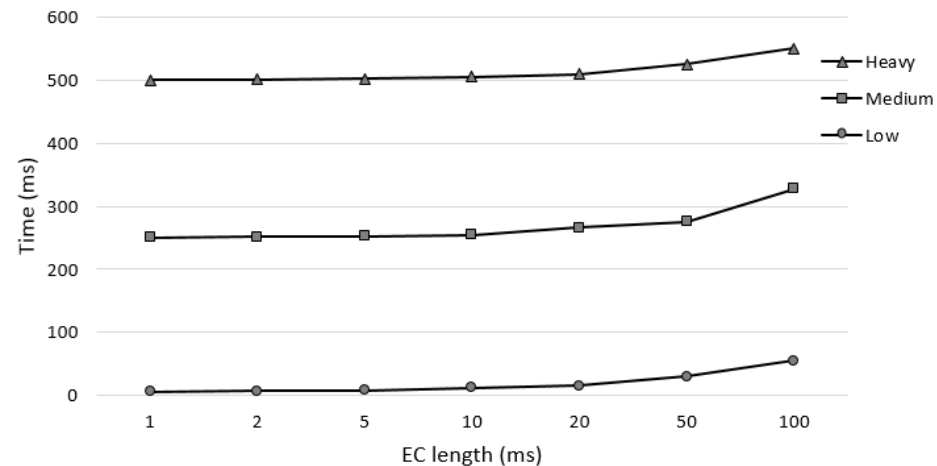
Experiments and Results

	Network Load (ms)			Concurrency (# nodes)
	Low	Medium	Heavy	
Test 1	1	50	100	1
Test 2	1	50	100	10

Test 1



Test 2



A First Performance Analysis of the Admission Control in the HaRTES Ethernet Switch

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Abstract

There is a growing interest in developing embedded systems capable of being deployed in dynamic environments that may change in unpredictable manners. When such systems are Distributed Embedded Systems (DESs) they must exhibit flexibility at all levels of their architecture, including the network. On the other hand, there is a clear trend in industry towards using Ethernet-based protocols at the network level of DESs.

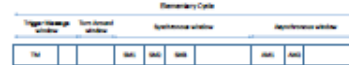
Nevertheless, Ethernet lacks appropriate support for real-time (RT) communications, mixing different RT traffic and on-line management of the Quality of Service (QoS). Several implementations of the Flexible Time-Triggered (FTT) protocol over Ethernet were proposed to cope with these drawbacks.

FTT is a master/slave protocol that is able to simultaneously convey real and non-real-time traffic and provides mechanisms for dynamically changing the QoS of the network, including Admission Control (AC). The AC is a fundamental component for on-line network management, since it guarantees that each participant gets the required QoS.

This paper presents the implementation in OMNeT++ of a simulation model of the AC in the FTT HaRTES switch as well as a preliminary performance study using that model.

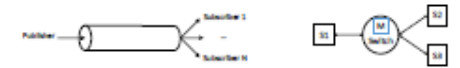
Flexible Time-Triggered

Flexible Time-Triggered supports event and time-triggered traffic in a flexible manner. Follows a master/slave architecture. The master organizes the communication in slots of fixed duration called Elementary Cycles, by sending the so-called Trigger Message to synchronise and trigger the communication among slaves.



The communication is carried out through virtual communication channels called message streams. First slaves ask for the creation of the stream and afterwards ask to attach as publisher or subscribers.

The selected architecture is HaRTES, that contains the master node embedded inside the switch.



Admission Control in HaRTES

Slave information is saved in the SRDB in master and the NREDBs in nodes.

To create a stream, slaves send a request to the master with the QoS information.

The master processes the request and updates the SRDB.

The master broadcast the result to the slaves through the command message.

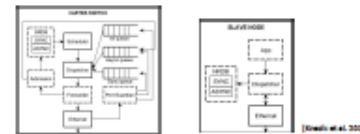
Slaves use the command message to update their NREDBs.



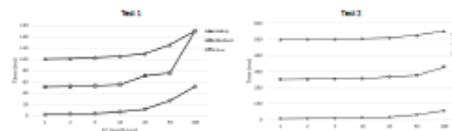
Modelling HaRTES' Admission Control and Quantitative Performance Analysis

OMNeT++ Model

Model of the HaRTES switch and a Slave node in OMNeT++. Dashed lines indicate modules affected by the Admission Control implementation.



Results



- Duration of the EC has a severe impact on the duration of the Admission Control.
- Level of concurrency impacts the duration of the Admission Control.
- Difficult for slaves to predict the duration of the Admission Control.

Experiments

Study the performance of the Admission Control. Specifically, study the impact of the EC length and the level of concurrency.

Test the performance under different load conditions, since the load of the network affects to the duration of the analysis carried out by the master.

Network with a single switch and ten slave nodes.

The table shows the parameters used in every test.

	Network Load (ms)			Concurrency (# nodes)
	Low	Medium	Heavy	
Test 1	1	50	100	1
Test 2	1	50	100	30

Conclusions and Future Work

Conclusions

- Study the impact of the EC length and level of concurrency on the performance of the Admission Control.
- One-hop network with a single switch and ten slave nodes.
- Considered several scenarios with different network loads.
- Difficult for slaves to determine the duration of the AC → Needed a confirmation for rejected requests to prevent further performance and reliability degradation.

Future work

- Extend the model to compare with the Admission Control of the FTT-GE architecture.
- Extend the comparison to include the Stream Reservation Protocol Implemented in Audio Video Bridging standard.

Questions?
Please meet me at
the poster!